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Digital System Design

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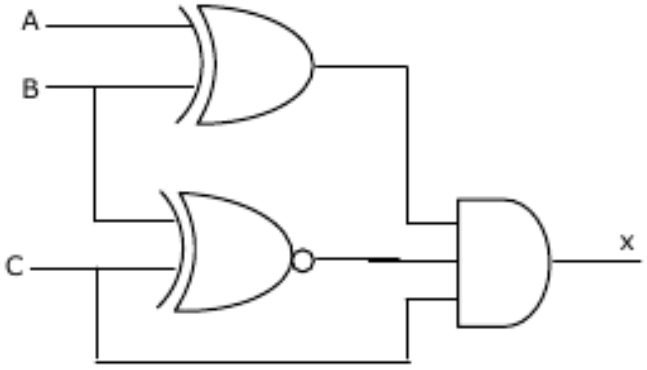
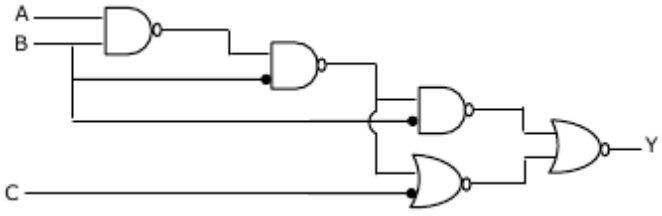
1 Boolean Algebra and Combinational Circuits

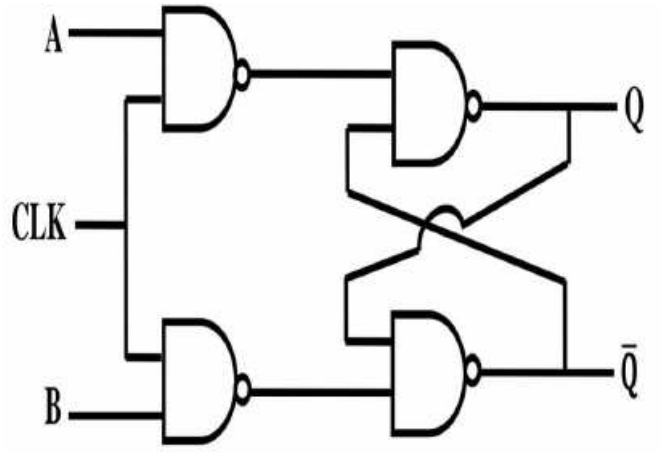
Problem 1.1. Find A, B, C such that $x = 1$.



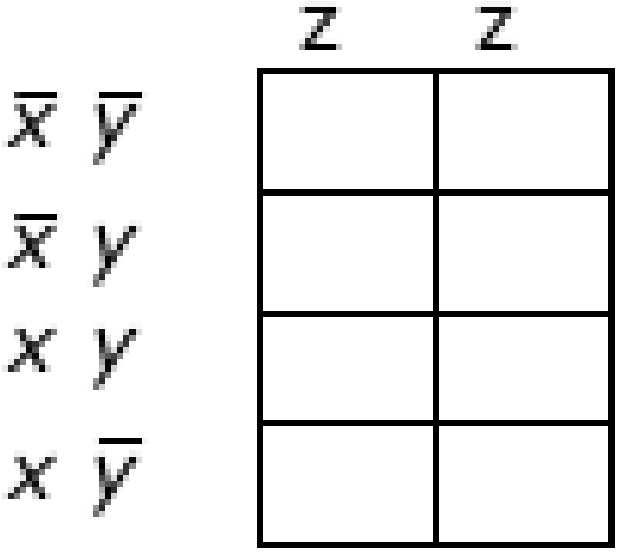
Problem 1.2. Express the output Y in terms of the inputs A, B and C



Problem 1.3. Write the truth table for the following circuit.



Problem 1.4. The operating conditions of 3 pumps, x, y, z (ON=1, OFF=0) are to be monitored. We want the output to be 1 whenever 2 of the 3 pumps fail (OFF). Use the following K-map to obtain the expression.



Problem 1.5. Write the truth table for 2-bit addition.

Problem 1.6. Express the number 17 in binary using 8 bits. Complement all the digits. Then add 1

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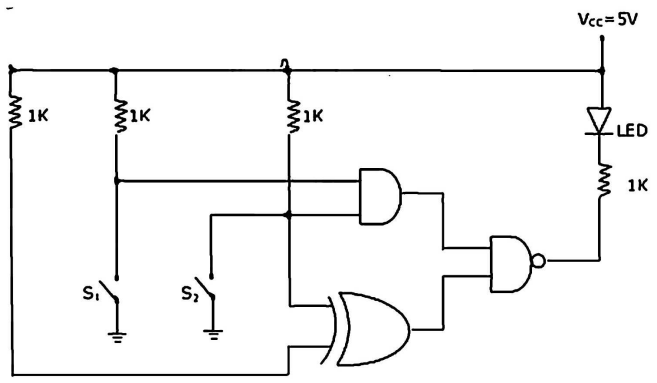
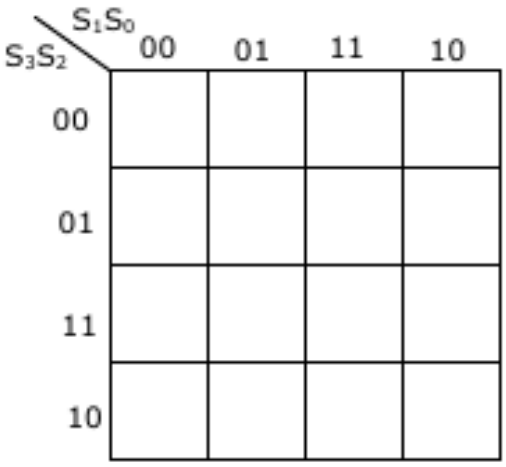
to this number. The binary number that you obtain is the two's complement of the number 17.

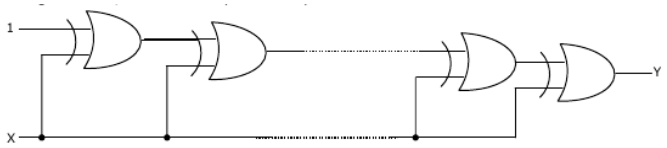
Problem 1.7. For what combination of the switches S_1 and S_2 will the LED glow?



Problem 1.8. For a digital block, $Y = f(S_3, S_2, S_1, S_0) = \sum m(1, 5, 6, 7, 11, 12, 13, 15)$. Use the following map to find the expression for Y.



Problem 1.9. Express Y in terms of X.

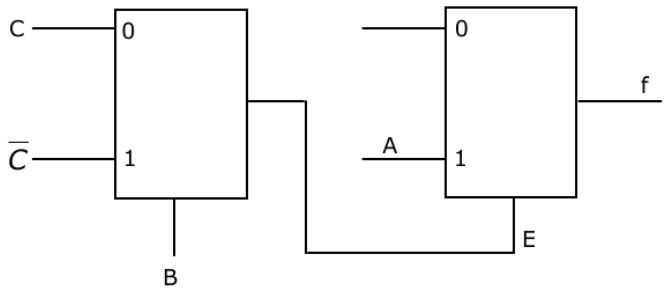


Problem 1.10. A one-bit full adder is to be implemented using 8-to-1 multiplexers (MUX).

1) Write the truth table for sum(S) and carry to the next stage (C_N) in terms of the two bits (A, B) and carry from the previous stage (C_p). The truth table should be in the ascending order of (A,B,C_p), i.e. (000,001,010,...etc.).
2) Implement S and C_N using 8-to-1 multiplexers.

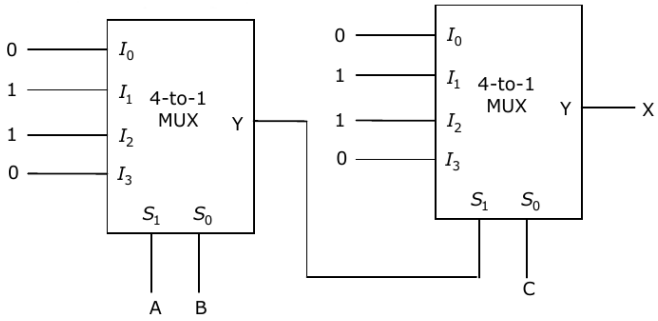
Problem 1.11. A Boolean function f of two variables x and y is defined as follows:
$f(0,0) = f(0,1) = f(1,1) = 1; f(1,0) = 0$
Assuming complements of x and y are not available, a minimum cost solution for realizing f using only 2-input NOR gates and 2-input OR gates (each having unit cost) find the total cost.

Problem 1.12. Write the Boolean function f implemented in figure using two input multiplexers



Problem 1.13. If $X = 01110$ and $Y = 11001$ are two 5-bit binary numbers represented in two's complement format. Find the sum of X and Y represented in two's complement format using 6 bits.

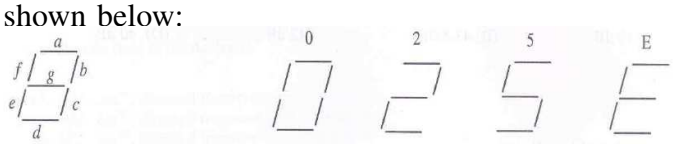
Problem 1.14. In the following circuit, find the expression for X.



Statement for the next two problems Two products are sold from a vending machine, which has two push buttons P_1 and P_2 when a button is pressed, the price of corresponding product is displayed in your seven segment display.

- if no buttons are pressed, '0' is dispalyed, signifying 'Rs.0'.
- if only P_1 is pressed, '2' is dispalyed, signifying 'Rs.2'.
- -if only P_2 is pressed, '5' is dispalyed, signifying 'Rs.5'.
- if both P_1 and P_2 are pressed, 'E' is dispalyed, signifying 'Error'.

The names seven segments in the 7-segment display, and the glow of display for '0', '2', '5' and 'E' are shown below:



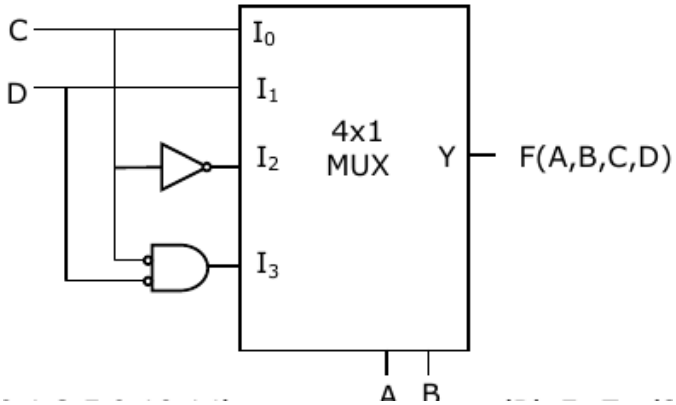
Consider

1) push button pressed/not pressed is equivalent to logic 1/0 respectively.
2) a segment glowing/not glowing in the display is equivalent to logic 1/0 respectively

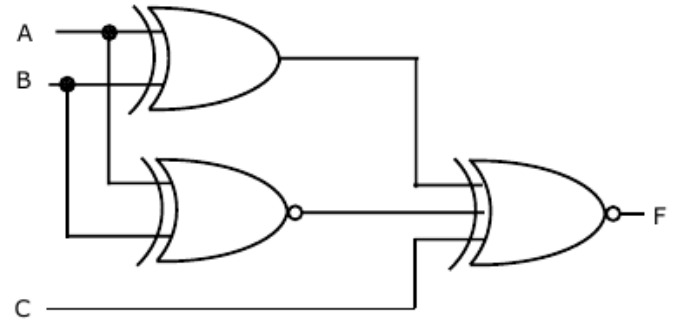
Problem 1.15. If segments a to g are considered as function of P_1 and P_2, then write the expression for g in terms of P_1 and P_2.

Problem 1.16. Design the logic of the driver for the 7-segment display.

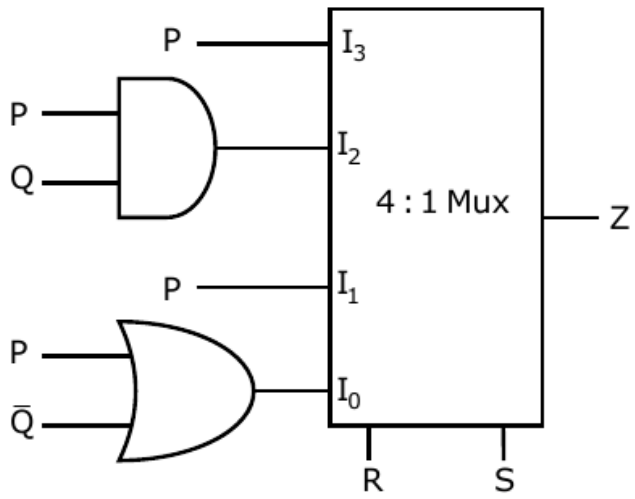
Problem 1.17. Find the boolean function realized by the logic circuit shown below:



Problem 1.18. For the output F to be 1 in the logic circuit shown, what will be the input combination?



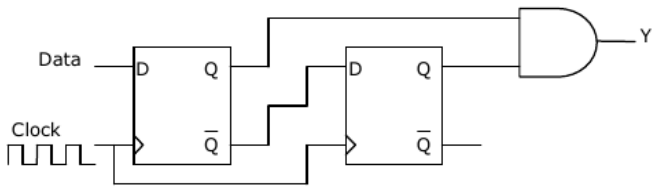
Problem 1.19. For the circuit shown in the following figure $I_0 - I_3$ are inputs to the 4:1 multiplexer R(MSB) and S are control bits. Write the expression for Z.



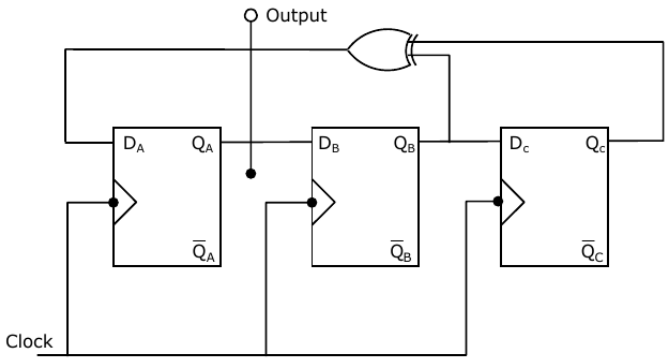
2 Sequential Circuits

Problem 2.1. Consider the circuit in Problem 1.3. Will the race around condition occur or not? Explain your answer.

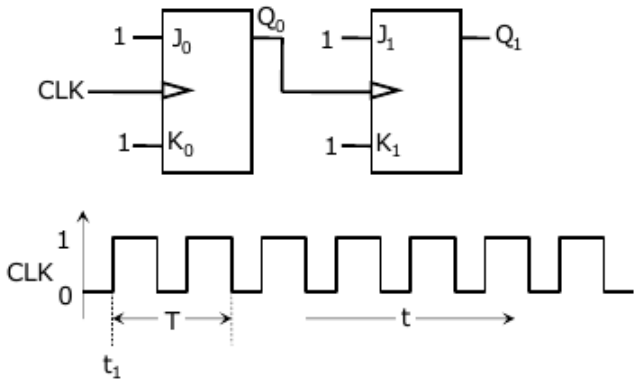
Problem 2.2. Let the Output Y in circuit below be '1'. Explain whether data D will change from 0 to 1 or 1 to 0



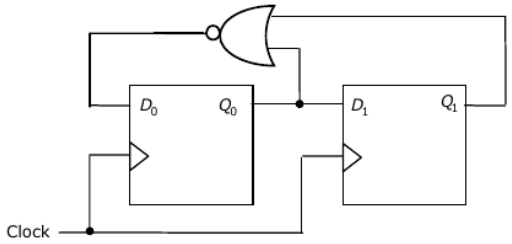
Problem 2.3. Assuming that flip-flops are in reset condition initially, What will be the count sequence at Q_A:



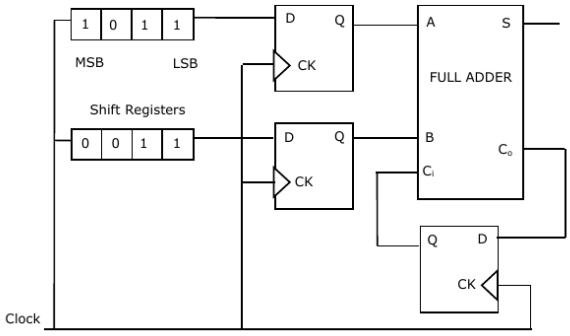
Problem 2.4. For each of the positive edge-triggered J-K flip flop used in the following figure, the propagation delay is dT. Plot the waveform for Q_1.



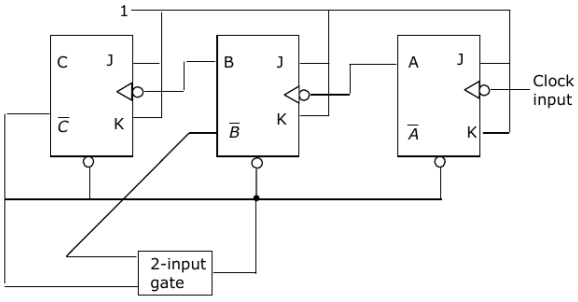
Problem 2.5. For the circuit shown below, find the counter state sequence for (Q_1 Q_0).



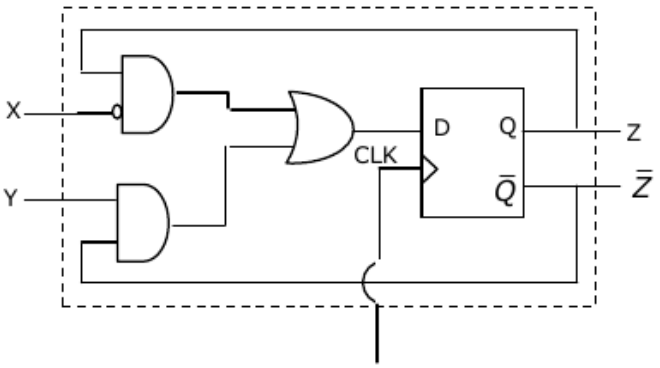
Problem 2.6. For the circuit shown in figure below, two 4-bit parallel-in serial-out shift registers loaded with the data shown are used to feed the data to a full adder. Initially, all the flip-flops are in clear state. After applying two clock pulses, what will be the outputs of the full-adder?



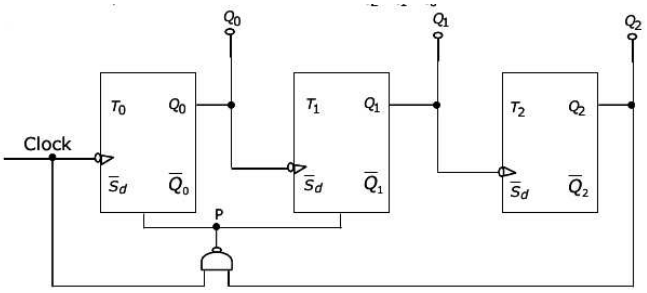
Problem 2.7. In the modulo-6 ripple counter shown in Figure, the output of the 2-input gate is used to clear the J-K flip-flops. What will be the logic gate for "2-input gate".



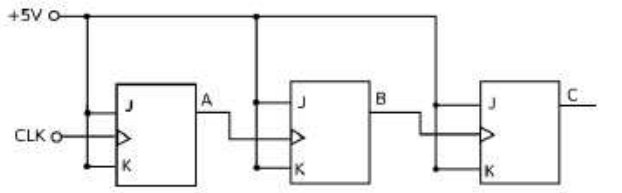
Problem 2.8. A sequential circuit using D flip-flop and logic gates is shown in figure below, where X and Y are the inputs and Z is the output. Explain type of flip-flop represented by the circuit.

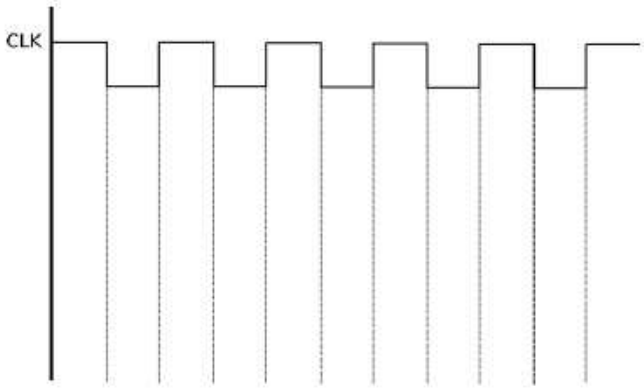


Problem 2.9. The counter shown in figure is initially in state $Q_2 = 0$, $Q_1 = 1$, $Q_0 = 0$. With reference to the CLK input, draw waveforms for Q_2, Q_1, Q_0 and P for the next three CLK.



Problem 2.10. In the circuit given , draw the waveform of A, B, C given the waveform of CLK . Explain how A, B, C represent the bits of a reverse counter. Also write the M SB and LSB of the number. Initially $A = B = C = 0$.

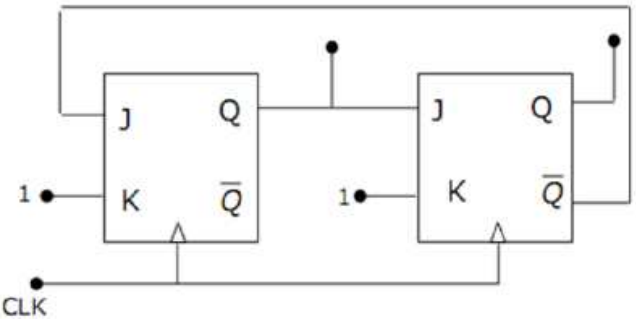




Problem 2.11. Implement a T flip-flop using an SR flip-flop, whose truth table is given below.

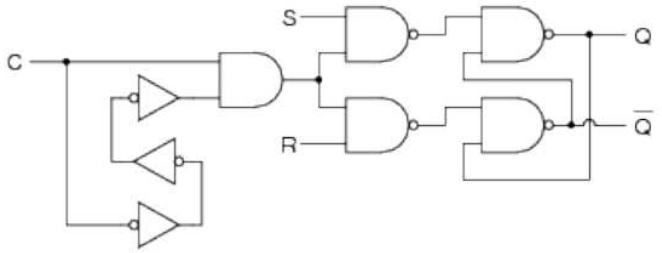
S	R	$Q(n+1)$
0	0	$Q(n)$
0	1	0
1	0	1
1	1	*

Problem 2.12. The given figure shows a counter. What is K is equal to?

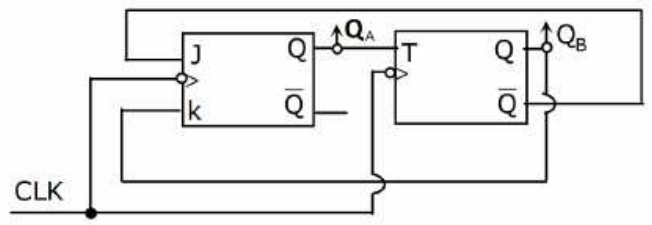


Problem 2.13. How many D-flip-flops are needed in a 7-state finite state machine?

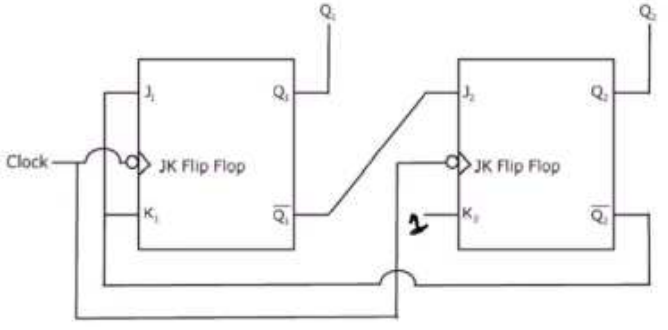
Problem 2.14. Explain how the addition of a propagation-delay-based one-shot circuit to the enable input of an S-R latch changes its behavior? Specifically, reference your answer to a truth table for this circuit.



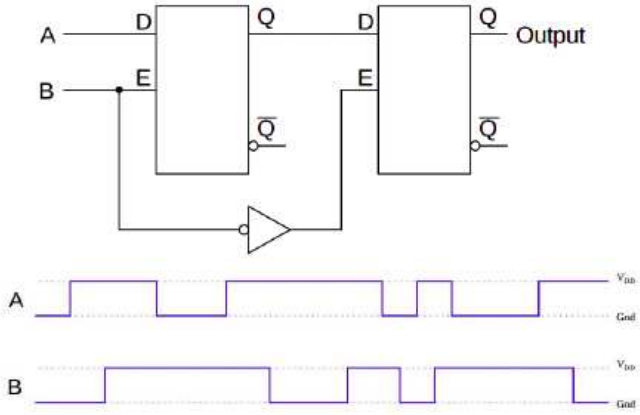
Problem 2.15. A two bit counter circuit is shown. If the state Q_A Q_B of the counter at the clock time T is 10 then the state Q_A Q_B of the counter at T+2(after two clock cycles) will be:



Problem 2.16. What are the counting stages (Q_1 and Q_2) for the counter shown in figure below?



Problem 2.17. Determine the final output states over time for the following circuit, built from D-type gated latches.


A
B
D
E
Q
$\overline{Q}$
D
E
Q
$\overline{Q}$
Output
A
B
V_{DD}
Gnd
V_{DD}
Gnd