

Programing FPGA using Vivado

Tanmay Agarwal, G V V Sharma*

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1 SOFTWARE SETUP

- 1) Vivado 2016.4 Software
- 2) Ubuntu 16.04 OS.

1.1 Steps to download Vivado

- 1) Go to Xilinx website and Create the Xilinx Account.
- 2) Open your Xilinx Account and go to the support section.
- 3) Under the support tag you will find Download & Licensing click on that.
- 4) From left hand side click on 2016.4 version.
- 5) Download the Linux self Extracting web installer file.The file will be .bin file.
- 6) Open the terminal and go to directory where the file is saved.
- 7) Run the .bin file in the terminal by using following commands .

```
sudo chmod +x file_name.bin
sudo ./file_name.bin
```

These command will run your file and an Vivado installer window will appear that will show the list of all the OS which software supports. Click on the next

- 8) It will ask for the Xilinx credentials. Just enter your Xilinx credentials and click on Download

and install. It will take some time for downloading and installation.

Note:- While downloading click on the boxes that it will ask for. In Linux vivado doesn't come with the Cable Drivers, you have to install it Manually.

1.2 Licensing



Fig. 1.0: VLM

- 1) After the installation one window will appear Vivado License Manager(VLM).In that Window click on Get free License Vivado free webpack SDK as shown in fig VLM
- 2) Click on save link as.
- 3) Now click on the link that you have saved. It will direct you to the License generating section in xilinx site. fig(License)

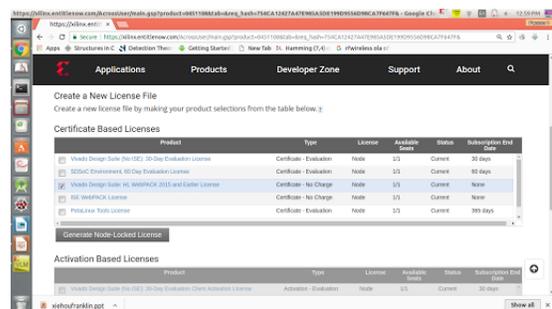


Fig. 1.0: License

- 4) In License window under the certificate based licenses select vivado design suite: HL webpack 2016 and Earlier License and click on Generate Node-Locked License.

*The author is with the Department of Electrical Engineering, Indian Institute of Technology, Hyderabad 502285 India e-mail: gadevall@iith.ac.in. All content in this manual is released under GNU GPL. Free and open source.



Fig. 2.0: Create

```

always @(posedge clk) begin
    delay = delay+1;
    if (delay==27'
        b101111101011110000100000000
    ) begin
        delay _<=_27'b0;
        A<=(!A);
    end
end
endmodule

```

- 9) After writing the code you have to mention the output port in the constraint file(XDC file for Zedboard.)You can download the XDC file from following link:
edboard.org/support/documentation/1521
- 10) Add the constraint file in the project by going to Add sources.
- 11) Add constrain
- 12) select the XDC file from where you have saved it.Click on finish.
- 13) Now make the changes in the XDC file according to Program.
- 14) change CCLK with clk and JA1 with A. clk is the clock that we have taken and A is the variable that we are using for blinking that will be connected to pmod JA.See the Pmod diagram.
- 15) Connect the JA1 with the Positive end of the Led and the Gnd to other end.
- 16) Now generate the bit stream by clicking on generate bit stream tag in left side of window.It will also ask for the synthesis click on ok.
- 17) After generating of bit stream it will ask for opening the implementation diagram click on cancel.
- 18) Now open the Hardware Manager and click on

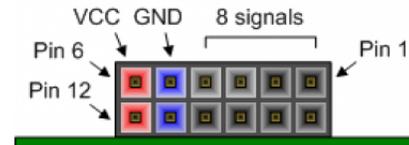
Fig. 16. Pmod Connectors
– front view as loaded on PCB.

Fig. 2.0: PMOD

target device and auto connect.

- 19) Select the board and the click on program device.
- 20) Observe the Output . Led will be Blinking.
Note:- Connect the usb to the jtag(Programming port).Also check the following:-
JP1 open.
JP2 shorted
JP3 shorted
JP6 shorted
JP7 connected to GND
JP8 connected to GND
JP9 connected to GND
JP10 connected to GND
JP11 connected to GND
JP12 (XADC) open
JP13 open
J21 (current sense) open
VADJ shorted at 1V8